REMARKS

This amendment is filed in response to the Office Action dated November 16, 2004. Applicants submit that this application should be allowed and the case passed to issue.

Care has been taken to avoid the introduction of new matter. The amendments to the specification are supported by the accompanying figures. Fig. 6 clearly discloses the source/drain regions formed sandwiching the dual-gate electrode 4. Figs. 10 and 11 clearly disclose the graphs illustrating junction leakage vs. applied voltage.

Claims 1-6 are pending in this application and were rejected.

Initially, it is noted that Young et al. (U.S. Patent No. 4,851,257) cited in the following rejection was not cited on a PTO-892. Applicant respectfully requests that the Examiner cite this reference on a PTO-892 in the next official action.

Claim Rejections Under 35 U.S.C. § 102

Claim 1 was rejected under 35 U.S.C. § 102(b) as being anticipated by Young et al. (U.S. Patent No. 4,851,257). This rejection is traversed, and reconsideration and withdrawal thereof respectfully requested. The following is a comparison between the invention, as claimed, and the cited prior art.

An aspect of the invention, per claim 1, is a semiconductor device comprising a semiconductor substrate having two types of active regions that are a PMOS region and an NMOS region separated from each other in plan view by a PN separation film. A dual-gate electrode extends linearly across the PMOS region, the PN separation film and the NMOS region collectively on an upper side of the semiconductor substrate. The dual-gate electrode includes a P-type portion positioned on the PMOS region, an N-type portion positioned on the NMOS region and a PN junction positioned between the P-type portion and the N-type portion. The

PN junction includes a silicide region subjected to silicidation. The silicide region is apart from both the PMOS region and the NMOS region and is formed within an area of the PN separation film in plan view.

The Examiner asserted that Young et al. teach a semiconductor device comprising a semiconductor substrate 10 having PMOS and NMOS regions separated by a PN separation film 20/420, a dual gate 72/212/451 extending linearly across the PMOS region, the PN separation film, and the NMOS region, and silicide regions 75/219.

The factual determination of lack of novelty under 35 U.S.C. § 102 requires the identical disclosure in a single reference of each element of a claimed invention, such that the identically claimed invention is placed into the recognized possession of one having ordinary skill in the art. *Dayco Prods., Inc. v. Total Containment, Inc.*, 329 F.3d 1358, 66 USPQ2d 1801 (Fed. Cir. 2003); *Crown Operations International Ltd. v. Solutia Inc.*, 289 F.3d 1367, 62 USPQ2d 1917 (Fed. Cir. 2002). There are significant differences between the claimed semiconductor device and the device disclosed by Young et al. that would preclude the factual determination that Young et al. identically describe the claimed invention within the meaning of 35 U.S.C. § 102.

Contrary to the Examiner's assertion, Young et al. do not disclose the dual gate electrode including a P-type portion positioned on the PMOS region and an N-type portion positioned on the NMOS region, as required by claim 1. Although, the Examiner alleged that Young et al. disclose a dual gate 72/212/451 extending linearly across the PMOS region, the PN separation film, and the NMOS region, and silicide regions 75/219, it is not seen where Young et al. disclose the asserted dual gate electrode extending as claimed.

Claims 1-3 are rejected under 35 U.S.C. § 102(b) as being anticipated by Liaw (U.S. Patent No. 6,214,656). This rejection is traversed, and reconsideration and withdrawal thereof respectfully requested.

The Examiner averred that Liaw teaches a semiconductor device comprising a semiconductor substrate 10 having PMOS and NMOS regions separated by a PN separation film 12, a dual gate 30/32 extending linearly across the PMOS region, the PN separation film, and the NMOS region, and silicide region 62.

Liaw, however, does not anticipate the instant claims because Liaw does not disclose that the silicide layer is placed apart from both the PMOS region and the NMOS region, as required by claim 1. Rather, Liaw teaches that the silicide layer 62 is adjacent to the PMOS and NMOS regions in plan view, as shown in FIG. 15. Furthermore, adverting to Figs. 7-10 and 14, the silicide layer of Liaw is formed beyond the area of the PN separation film, not **within** an area of the PN separation film, as required by claim 1.

The factual determination of lack of novelty under 35 U.S.C. § 102 requires the disclosure in a single reference of each element of a claimed invention. *Helifix Ltd. v. Blok-Lok Ltd.*, 208 F.3d 1339, 54 USPQ2d 1299 (Fed. Cir. 2000); *Electro Medical Systems S.A. v. Cooper Life Sciences, Inc.*, 34 F.3d 1048, 32 USPQ2d 1017 (Fed. Cir. 1994); *Hoover Group, Inc. v. Custom Metalcraft, Inc.*, 66 F.3d 399, 36 USPQ2d 1101 (Fed. Cir. 1995); *Minnesota Mining & Manufacturing Co. v. Johnson & Johnson Orthopaedics, Inc.*, 976 F.2d 1559, 24 USPQ2d 1321 (Fed. Cir. 1992); *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051 (Fed. Cir. 1987). Because Young et al. do not disclose the dual gate electrode including a P-type portion positioned on the PMOS region and an N-type portion positioned on the NMOS region, and Liaw does not disclose the silicide region is apart from both the PMOS and the

NMOS region and is formed within an area of the PN separation film in plan view, as required by claim 1, Young et al. and Liaw do not anticipate claim 1.

Applicants further submit Young et al. and Liaw, whether taken alone, or in combination do not suggest the claimed semiconductor device.

Claim Rejections Under 35 U.S.C. § 103

Claims 1-6 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Liaw in view of Goto (U.S. Patent No. 5,902,121). This rejection is traversed, and reconsideration and withdrawal thereof respectfully requested.

The Examiner asserted that Liaw substantially teaches the claimed invention but Liaw does not show a contact to active region overlapping the dual gate. The Examiner relied on Goto's teaching of contacts overlapping gate patterns and concluded that one of ordinary skill in this art would have been motivated to substitute the overlapping contacts in order to enhance the margin of alignment.

The combination of Goto et al. with Liaw, however, does not suggest the claimed semiconductor device because Goto et al. do not cure the deficiencies of Liaw. Goto et al. do not suggest the silicide region is apart from both the PMOS and the NMOS region and is formed within an area of the PN separation film in plan view, as required by claim 1. Therefore, the instant claims would not have been obvious in view of the teachings of Goto et al. and Liaw.

The dependent claims are allowable for at least the same reasons as claim 1 and further distinguish the claimed invention.

In light of the above Remarks, this application should be allowed and the case passed to issue. If there are any questions regarding these remarks or the application in general, a

telephone call to the undersigned would be appreciated to expedite prosecution of the application.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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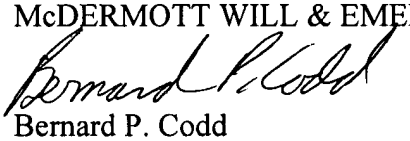

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